CLAIMS

1. A signal balancing circuit for capacitively coupled signaling between transmitting and receiving devices both receiving a synchronizing clock signal, the signal balancing system comprising:

a plurality of capacitively coupled signal lines on which data signals are transmitted from the transmitting device to the receiving device, the data signals representing streams of binary data having a data interval to which each binary digit corresponds;

an encode circuit having an output at which a balancing signal is provided, the encode circuit coupled to each capacitively coupled signal line to monitor each data signal over a respective time interval for a change in logic states, the encode circuit inverting a data signal for a data interval in response to the data signal maintaining the same logic state throughout the time interval and further generating a balancing signal having a logic level and a timing relative to the time intervals of the respective data signals indicative of inversion of a particular data signal; and

a decode circuit coupled to the encode circuit to receive the balancing signal and further coupled to the capacitively coupled signal lines to invert the data signals for the data interval according to the logic level and timing of the balancing signal.

2. The signal balancing system of claim 1 wherein the decode circuit is capacitively coupled to the encode circuit to receive the balancing signal.

3. The signal balancing system of claim 1 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit monitors each data signal over a time interval of n data intervals for a signal transition.

4. The signal balancing system of claim 1 wherein the plurality of capacitively coupled signal lines comprises n signal lines, n being a multiple of eight, and the

encode circuit monitors each data signal over a time interval of eight data intervals for a signal transition.

5. The signal balancing system of claim 1 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit monitors each data signal over a time interval of (n+1) data intervals for a signal transition.

6. The signal balancing system of claim 5 wherein the encode circuit monitors each data signal over respective time intervals that are staggered by one data interval with respect to one another.

7. The signal balancing system of claim 5 wherein the decode circuit is capacitively coupled to the encode circuit to receive the balance signal and the encode circuit generates a balance signal having a signal transition following every n data intervals.

8. The signal balancing system of claim 1 wherein the synchronizing clock signal is capacitively coupled between the transmitting and receiving devices.

9. The signal balancing system of claim 1, further comprising a plurality of output buffers and input buffers coupled to the plurality of capacitively coupled signal lines, and wherein the output buffers and encode circuit are integrated with the transmitting device and the input buffers and the decode circuit are integrated with the receiving device.

10. A signal balancing system for capacitively coupled data signaling between a transmitting device and a receiving device both receiving a synchronizing clock signal, the signal balancing system comprising:

a plurality of output buffers for driving a corresponding plurality of data signals;

a corresponding plurality of input buffers for receiving the plurality of data signals;

a corresponding plurality of capacitively coupled signal lines coupled between the output buffers and the input buffers on which the plurality of data signals are transmitted from the transmitting device to the receiving device;

an encode circuit having an output at which a balance signal is provided and coupled to each of the capacitively coupled signal lines to monitor each data signal for a signal transition occurring within repeating and non-overlapping time intervals, the repeating time intervals for each of the data signals equal in length of time and equally staggered with respect to one another over the length of time of one time interval, the encode circuit further coupled to each of the plurality of output buffers to cause a data signal to be inverted prior to transmission in the event the respective data signal does not change logic states over an immediately preceding time interval and generate a balance signal at a time and having a first logic level indicative of whether a data signal has been inverted and which of the plurality of data signals was inverted; and

a decode circuit coupled to the encode circuit to receive the balance signal and further coupled to each of the input buffers to cause an input buffer to invert the respective data signal received from the transmitting device in response to receiving the balance signal having the first logic level at the time corresponding to the inverted data signal.

11. The signal balancing system of claim 10 wherein the decode circuit is capacitively coupled to the encode circuit to receive the balance signal.

12. The signal balancing system of claim 10 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit monitors each data signal over a time interval of n bit intervals for a signal transition.

13. The signal balancing system of claim 10 wherein the plurality of capacitively coupled signal lines comprises n signal lines, n being a multiple of eight, and the encode circuit monitors each data signal over a time interval of eight bit intervals for a signal transition.

14. The signal balancing system of claim 10 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit monitors each data signal over a time interval of (n+1) bit intervals for a signal transition.

15. The signal balancing system of claim 14 wherein the encode circuit monitors each data signal over respective time intervals that are staggered by one bit interval with respect to one another.

16. The signal balancing system of claim 14 wherein the decode circuit is capacitively coupled to the encode circuit to receive the balance signal and the encode circuit generates a balance signal having a signal transition following every n bit intervals.

17. The signal balancing system of claim 10 wherein the synchronizing clock signal is capacitively coupled between the transmitting and receiving devices.

18. The signal balancing system of claim 10 wherein the output buffers and encode circuit are integrated with the transmitting device and the input buffers and the decode circuit are integrated with the receiving device.

19. A system in package (SiP) device, comprising:

a first device having a clock terminal to which a clock signal is applied and further having a first plurality of data terminals;

a second device having a clock terminal to which the clock signal is applied and further having a second plurality of data terminals;

a plurality of capacitively coupled signal lines coupled to the first and second plurality of data terminals on which data signals are transmitted between the first and second devices; and

a signal balancing circuit for capacitively coupled signaling between the first and second devices, the signal balancing system comprising:

an encode circuit having an output at which a balancing signal is provided, the encode circuit coupled to each capacitively coupled signal line to monitor each data signal over a respective time interval for a change in logic states, the encode circuit inverting a data signal for a data interval in response to the data signal maintaining the same logic state throughout the time interval and further generating a balancing signal having a logic level and a timing relative to the time intervals of the respective data signals indicative of inversion of a particular data signal; and

a decode circuit coupled to the encode circuit to receive the balancing signal and further coupled to the capacitively coupled signal lines to invert the data signals for the data interval according to the logic level and timing of the balancing signal.

20. The SiP device of claim 19 wherein the decode circuit of the signal balancing circuit is capacitively coupled to the encode circuit to receive the balancing signal.

21. The SiP device of claim 19 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit of the signal balancing system monitors each data signal over a time interval of n data intervals for a signal transition.

22. The SiP device of claim 19 wherein the plurality of capacitively coupled signal lines comprises n signal lines, n being a multiple of eight, and the encode circuit of the

signal balancing system monitors each data signal over a time interval of eight data intervals for a signal transition.

23. The SiP device of claim 19 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit of the signal balancing system monitors each data signal over a time interval of (n+1) data intervals for a signal transition.

24. The SiP device of claim 23 wherein the encode circuit of the signal balancing system monitors each data signal over respective time intervals that are staggered by one data interval with respect to one another.

25. The SiP device of claim 23 wherein the decode circuit of the signal balancing system is capacitively coupled to the encode circuit to receive the balance signal and the encode circuit generates a balance signal having a signal transition following every n data intervals.

26. The SiP device of claim 19 wherein the clock signal is capacitively coupled between the transmitting and receiving devices.

27. The SiP device of claim 19 wherein the signal balancing system further comprises a plurality of output buffers and input buffers coupled to the plurality of capacitively coupled signal lines, and wherein the output buffers and encode circuit are integrated with the transmitting device and the input buffers and the decode circuit are integrated with the receiving device.

28. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices;

a memory device coupled to the processor; and

a system in package (SiP) device coupled to the processor, the SiP device comprising:

a first device having a clock terminal to which a clock signal is applied and further having a first plurality of data terminals;

a second device having a clock terminal to which the clock signal is applied and further having a second plurality of data terminals;

a plurality of capacitively coupled signal lines coupled to the first and second plurality of data terminals on which data signals are transmitted between the first and second devices; and

a signal balancing circuit for capacitively coupled signaling between the first and second devices, the signal balancing system comprising:

an encode circuit having an output at which a balancing signal is provided, the encode circuit coupled to each capacitively coupled signal line to monitor each data signal over a respective time interval for a change in logic states, the encode circuit inverting a data signal for a data interval in response to the data signal maintaining the same logic state throughout the time interval and further generating a balancing signal having a logic level and a timing relative to the time intervals of the respective data signals indicative of inversion of a particular data signal; and

a decode circuit coupled to the encode circuit to receive the balancing signal and further coupled to the capacitively coupled signal lines to invert the data signals for the data interval according to the logic level and timing of the balancing signal.

29. The computer system of claim 28 wherein the decode circuit of the signal balancing circuit is capacitively coupled to the encode circuit to receive the balancing signal.

30. The computer system of claim 28 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit of the signal balancing system monitors each data signal over a time interval of n data intervals for a signal transition.

31. The computer system of claim 28 wherein the plurality of capacitively coupled signal lines comprises n signal lines, n being a multiple of eight, and the encode circuit of the signal balancing system monitors each data signal over a time interval of eight data intervals for a signal transition.

32. The computer system of claim 28 wherein the plurality of capacitively coupled signal lines comprises n signal lines and the encode circuit of the signal balancing system monitors each data signal over a time interval of (n+1) data intervals for a signal transition.

33. The computer system of claim 32 wherein the encode circuit of the signal balancing system monitors each data signal over respective time intervals that are staggered by one data interval with respect to one another.

34. The computer system of claim 32 wherein the decode circuit of the signal balancing system is capacitively coupled to the encode circuit to receive the balance signal and the encode circuit generates a balance signal having a signal transition following every n data intervals.

35. The computer system of claim 28 wherein the clock signal is capacitively coupled between the transmitting and receiving devices.

36. The computer system of claim 28 wherein the signal balancing system further comprises a plurality of output buffers and input buffers coupled to the plurality of

capacitively coupled signal lines, and wherein the output buffers and encode circuit are integrated with the transmitting device and the input buffers and the decode circuit are integrated with the receiving device.

37. A method of balancing a plurality of capacitively coupled data signals, comprising:

monitoring each of the data signals for a signal transition over respective repeating non-overlapping time intervals, the time intervals for each data signal staggered in time relative to one another over a time interval;

inverting a data signal for a data interval in response to the data signal maintaining a logic level throughout the respective time interval;

generating a balancing signal having a logic level and timing relative to the time intervals of the respective data signals indicative of inversion of a data signal for a data interval; and

inverting inverted data signals for the data interval in accordance with the balancing signal.

38. The method of claim 37 wherein monitoring each of the data signals for a signal transition over respective repeating non-overlapping time intervals comprises monitoring each of n data signals over time intervals of n data intervals.

39. The method of claim 37 wherein monitoring each of the data signals for a signal transition over respective repeating non-overlapping time intervals comprises monitoring each of n data signals over time intervals of (n+1) data intervals.

40. The method of claim 39 wherein generating a balancing signal comprises generating a balancing signal having a signal transition following every n data intervals.

41. A method for balancing a plurality of data signals on a corresponding plurality of capacitively coupled data lines, the method comprising:

evaluating the data signals for signal transitions occurring within a respective time interval, each data signal have a time interval of equal time and staggered in time with respect to the time intervals of the other signals;

where a data signal maintains the same logic level for the time interval, forcing a signal transition of the data signal from an original logic level to a complementary logic level and generating a balance signal having a logic level and timing with respect to the time interval of the data signal indicative of the forced transition of the particular data signal; and

forcing a transition of the transitioned signal at the appropriate time in accordance with the balance signal to recover the original logic level of the data signal.

42. The method of claim 41 wherein evaluating the data signals for a signal transitions occurring within a respective time interval comprises monitoring each of n data signals over respective time intervals of n bit intervals.

43. The method of claim 41 wherein evaluating the data signals for a signal transitions occurring within a respective time interval comprises monitoring each of n data signals over respective time intervals of (n+1) bit intervals.

44. The method of claim 43 wherein generating a balancing signal comprises generating a balancing signal having a signal transition following every n data intervals.